

LCFC Confidential

HS45A/HS55A(NMD461) MB Schematics Document

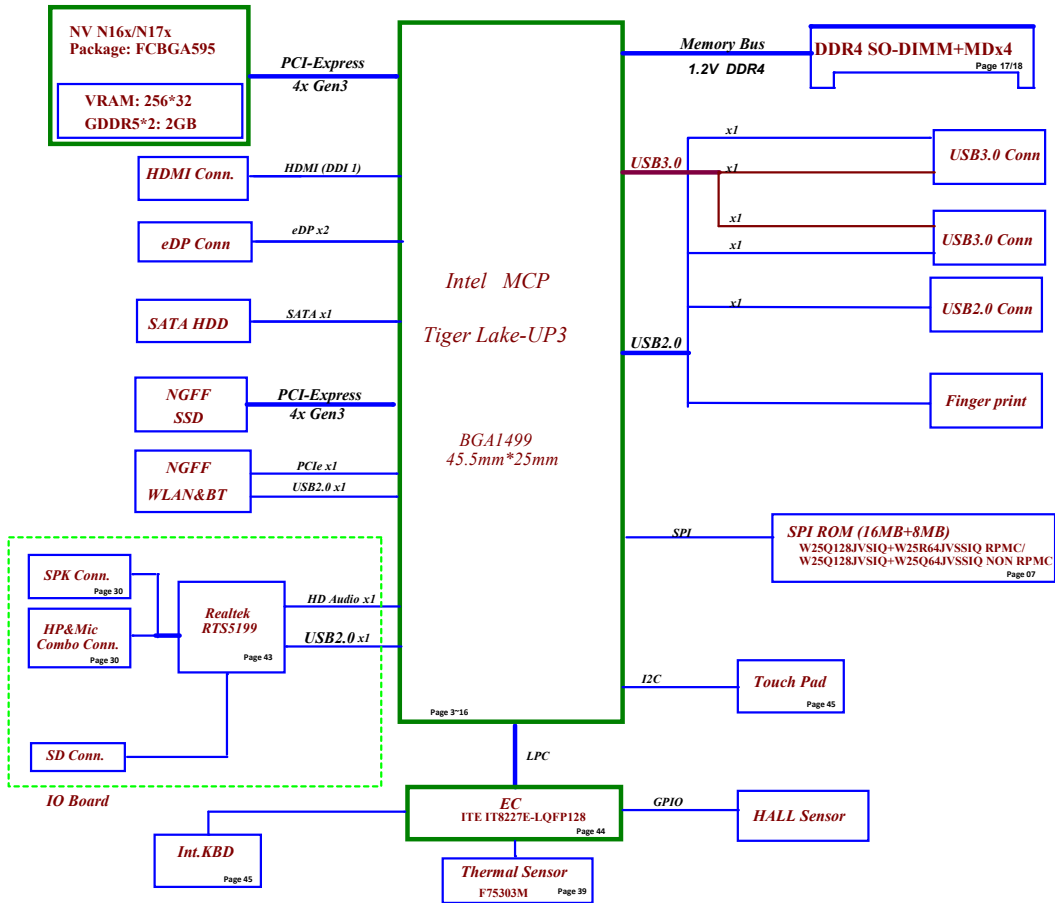
TGL UP3 with DDR4

2020-04

REV: 0.1

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Issued Date	2015/08/20	Deciphered Date	2016/08/20	
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V9B+	+3VALW +5VALW +3VALW_PCH +1.8VALW VCC_AUX	+1.2V +2.5V_DDR +VCCST +VCCSTG	+5VB +3VB +1.8VB +CPU_CORE +0.6VB
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8227E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WIMAX
EC_SMB_CK1 EC_SMB_DA1	IT8227E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8227E +3VS	X	X	V +3VC_AON	V +3VS	X	X	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8227E +3VAWL	X	X	X	V	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALN_PCH	X	X	X	X	X	V +3VALN_PCH	X	V +3VS	X	X


EC SMBus1 address		EC SMBus2 address		EC SMBus3 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100ab	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	DGPU	need to update				

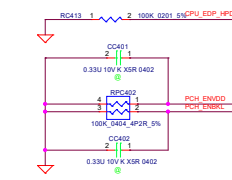
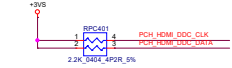
SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALN	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 NC
	4 NC
	5
USB2.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 NC
	4 NC
	5 Camera
	6 Touch screen
	7 Finger Print
	8 Card Reader
	9 USB2.0 conn
	10 Bluetooth
PCIE	5-8 X4 DGPU
	9 WLAN
	10 NC
	11 SATA HDD
	12 NC
	13-16 X4 PCIE/SATA SSD


BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
CD@	For cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME part
UMA@	For UMA part
OPT@	For NV GPU part
OPTN16@	For NV N168-GTR GPU part
OPTN17@	For NV N178-G1 GPU part
TSE	For touch screen part
TP@	For Touch Pad Part

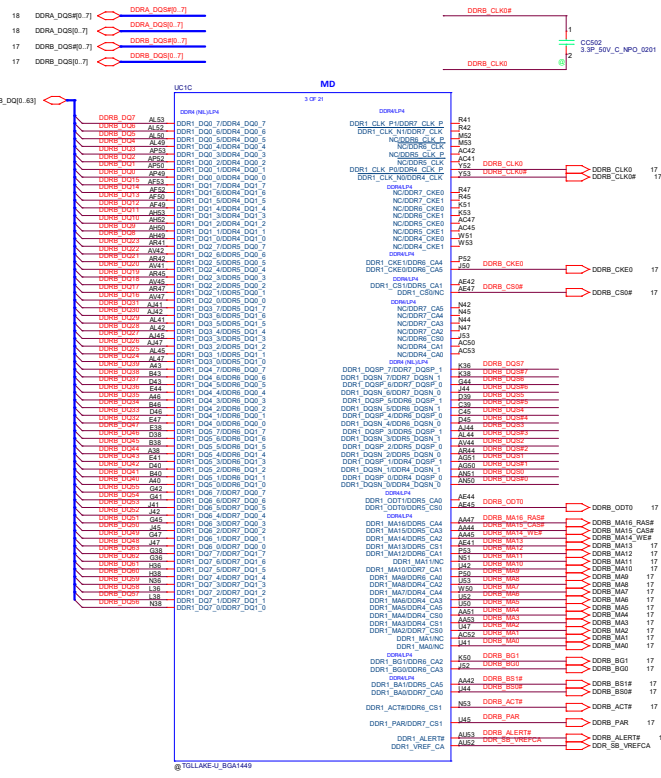
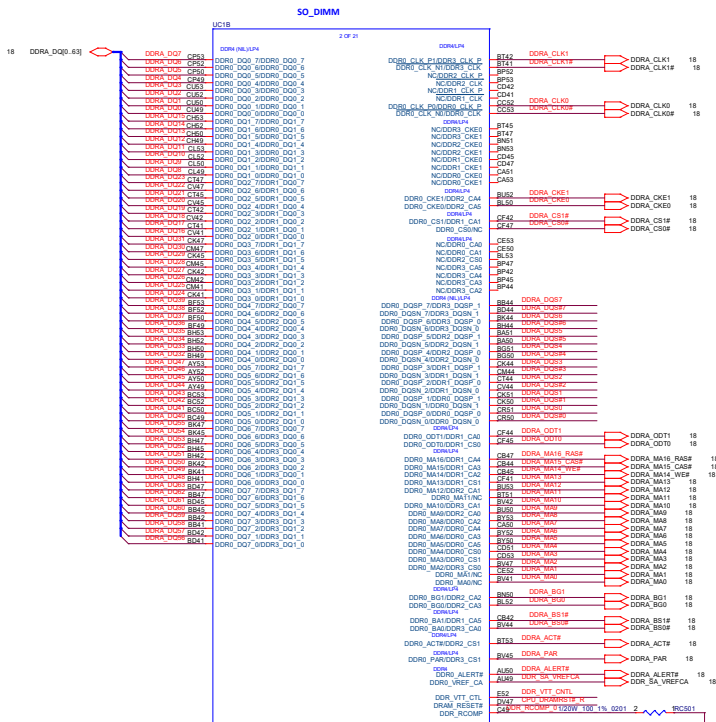
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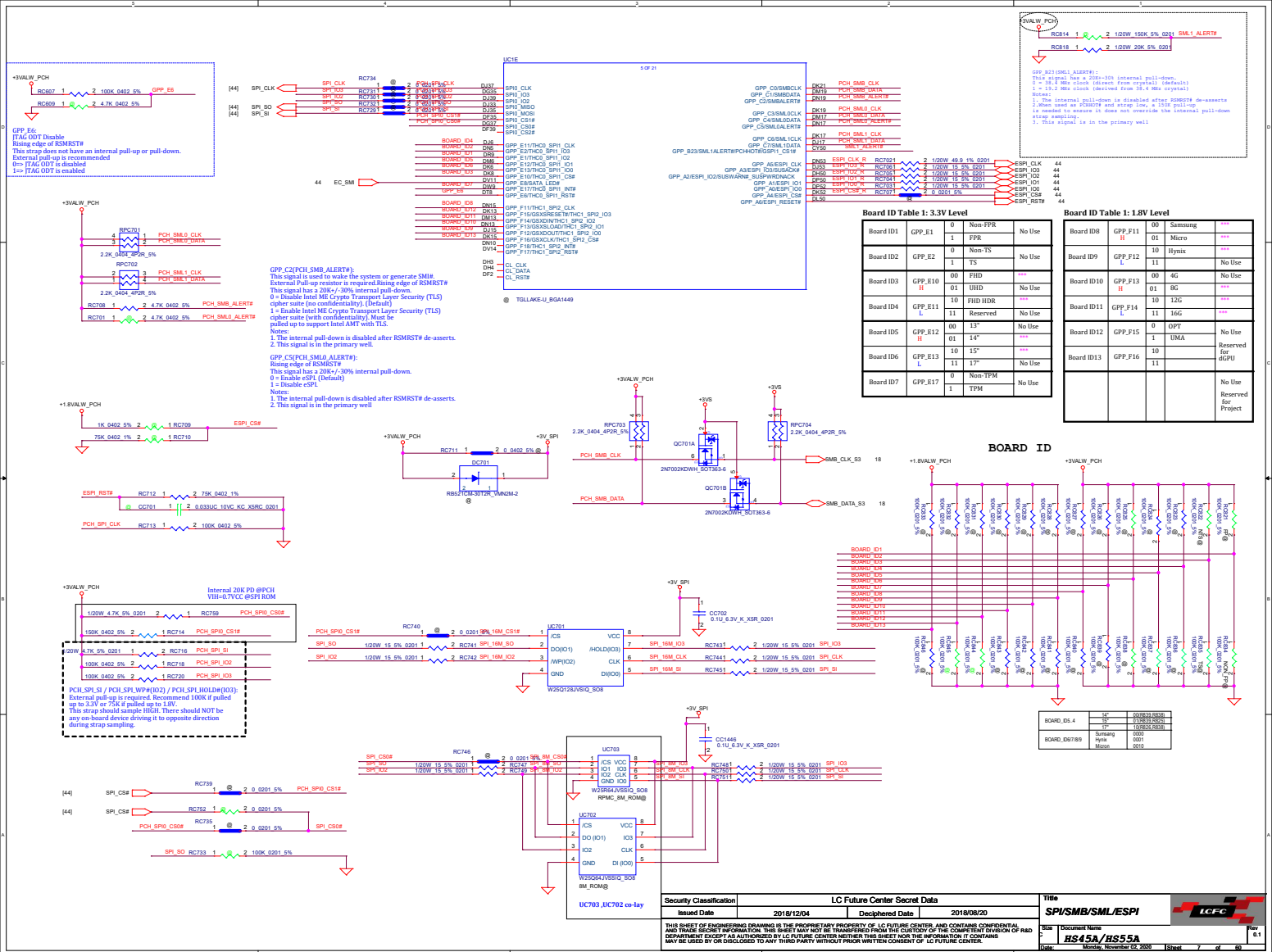


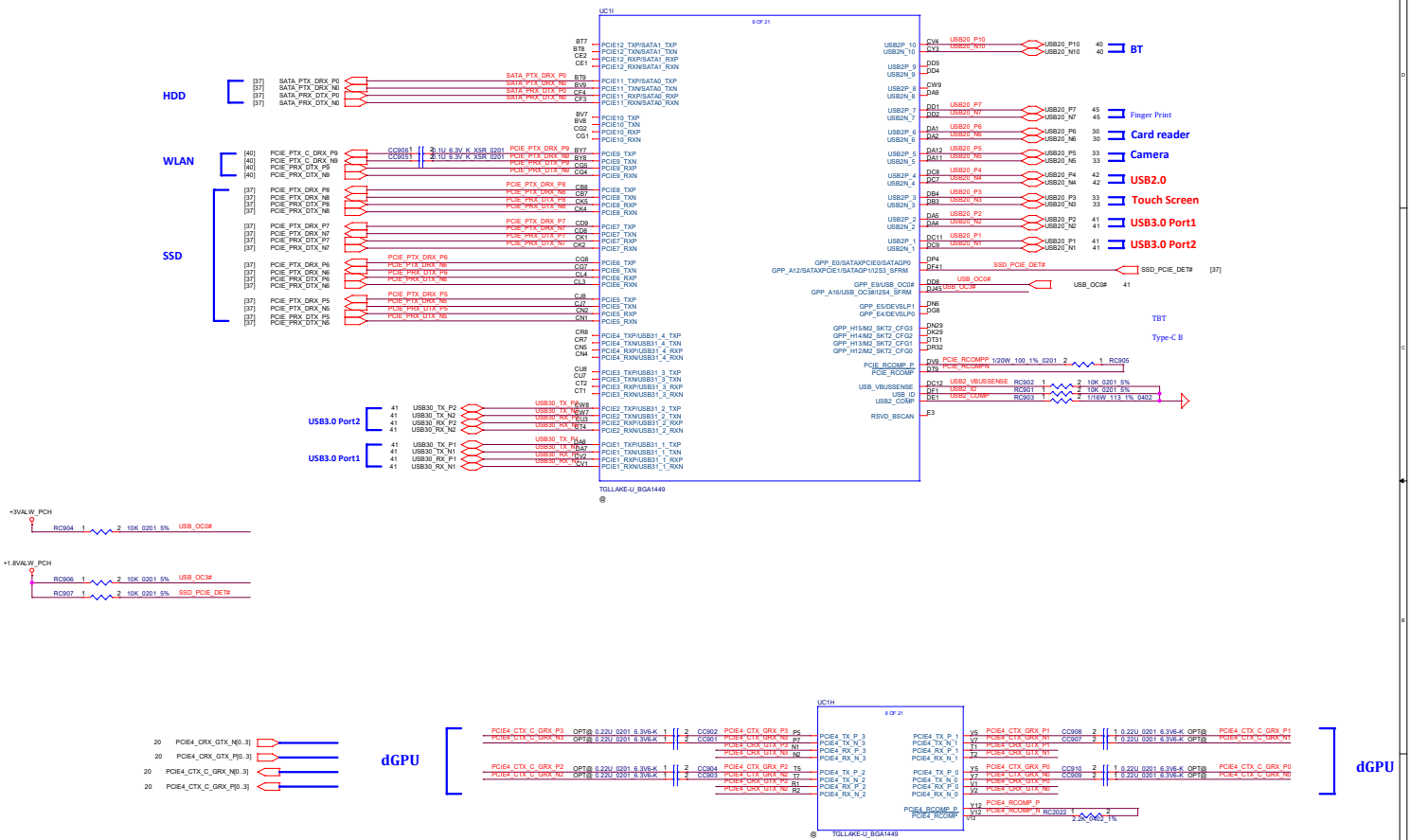
GPIO Group	Power Supply
GPP_A	1.8V
GPP_B/C/D/E	3.3V
GPP_F	1.8V(only)
GPP_G/H	3.3V
GPP_R/S	1.8V
GPD	3.3V(only)

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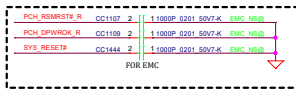
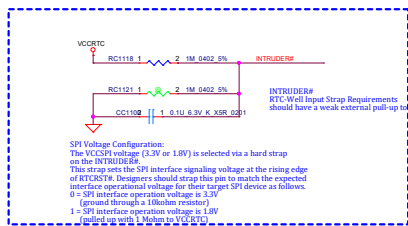
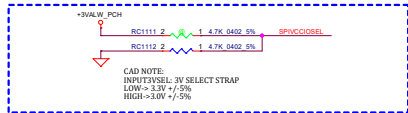
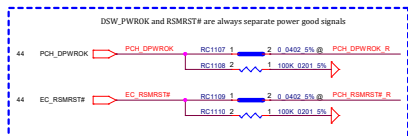


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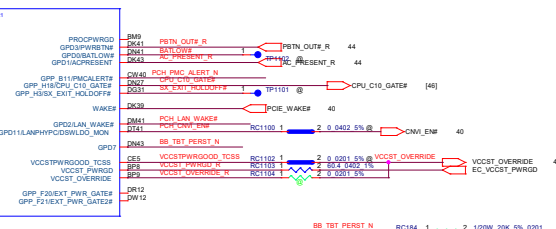
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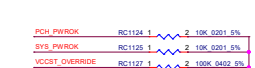
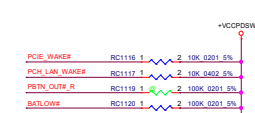
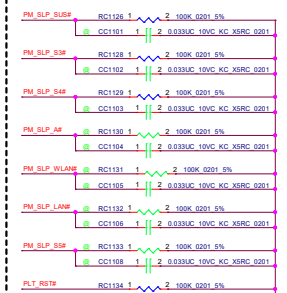
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TOLLAKE-U, BGA449

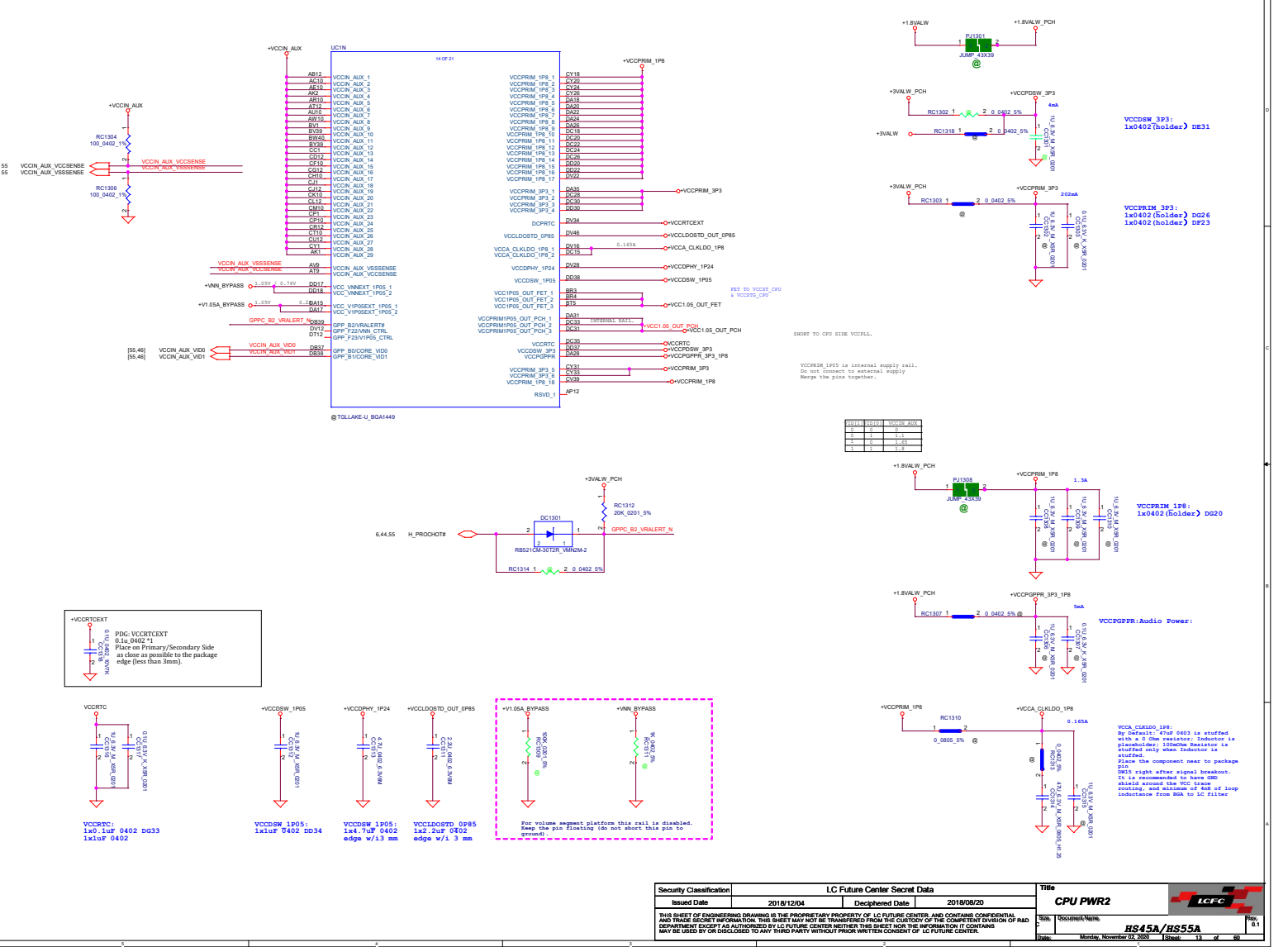



Glitch Free Requirements:
Pull-up resistor is required if a device is monitoring SLP_S0#
before RSMRSTW de-assertion
100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode

Glitch Free Requirements:
Cap or pull-down resistor is required
Option 1: Cap Implementation
330 nF for 2.5V Ramp Rate from 5-50ms
33 nF for 3.3V Ramp Rate Less than 5ms
Option 2: Pull-down Resistor Implementation
100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode



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VDDQ_CPU :

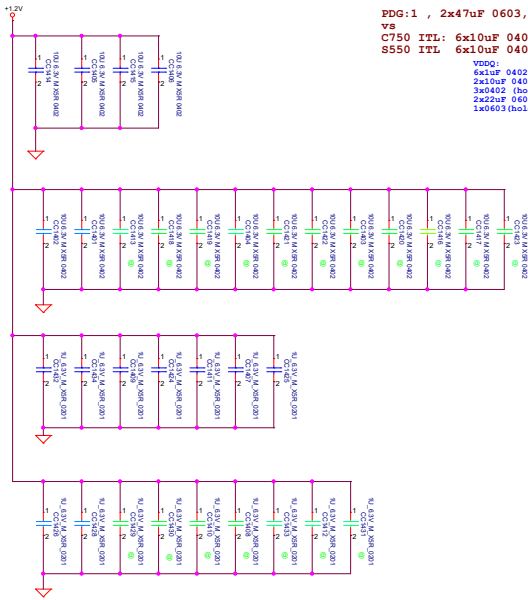
FDG:1 , 2x47uF 0603, 8x10uF 0402, 8x1uF 0402,

Vs

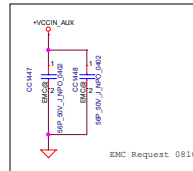
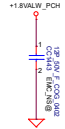
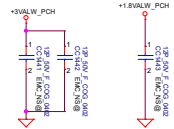
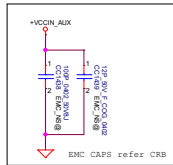
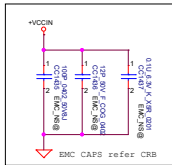
C750 ITL: 6x10uF 0402, 3x1uF 0402,10x1uF 0201,Reserve 8x10uF 0402,7x1uF 0201

S550 ITL: 6x10uF 0402, 9x1uF 0201 Reserve 11x10uF 0402, 7x1uF 0201

VDDQ:
5x1uF 0402 Back Outer row
2x10uF 0402 back Outer row
3x0402 (holder) back Outer row
2x22uF 0603 (ESD1MM need)
1x0603(holder)

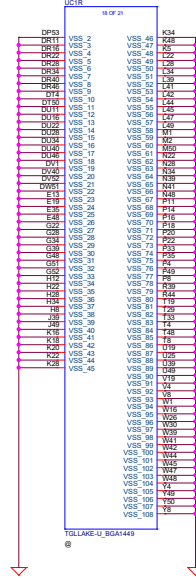
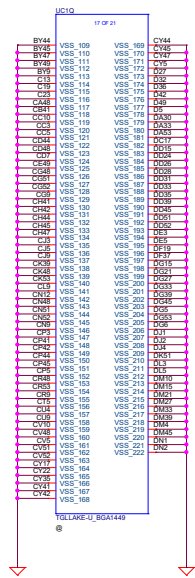
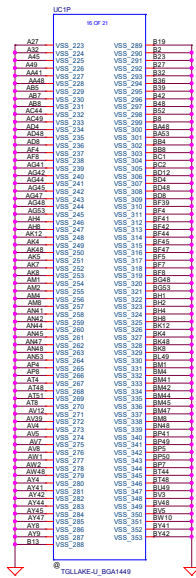


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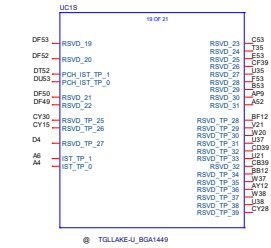
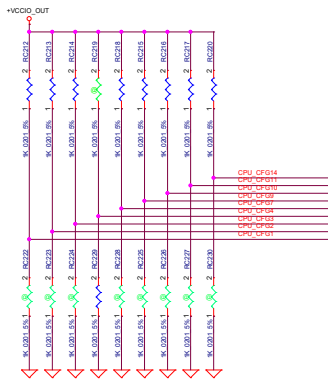


EMC Request 0810

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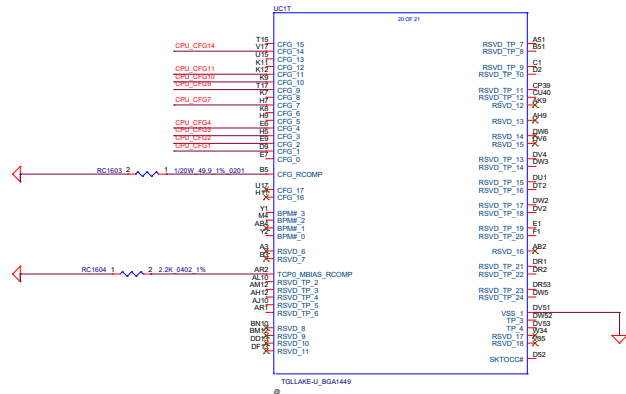



Change CFG Follow PDG_V1.0--Xohm1220

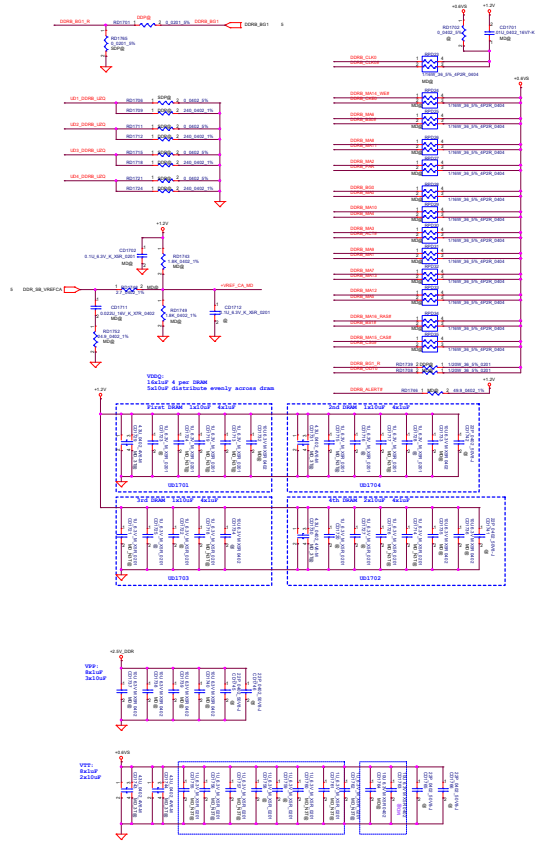
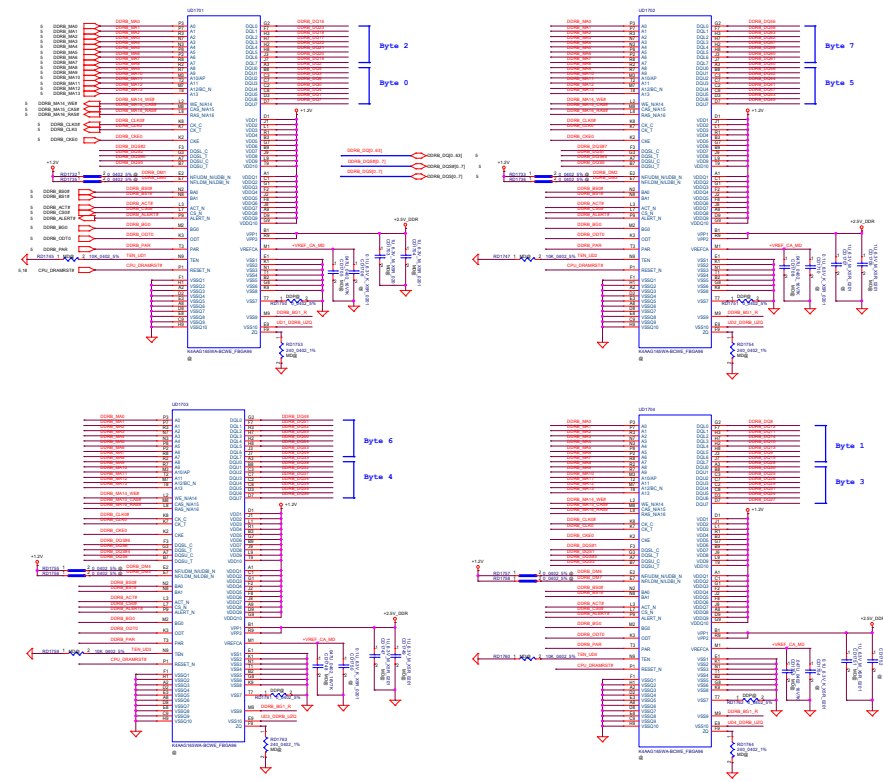
Pin Name	Strap Description	Configuration	Default Value
CFG[0]	RSVD	None	
CFG[3:1]	RSVD	Pull-up to VCCIO	1Kohm
CFG[4]	eTP enable strap 1 = Disabled 0 = Enabled	Pull-up to VCCIO / Pull-down Platform design dependent	1Kohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training 1 = (default) PEG Train immediately following RSTn# de-assertion. 0 = PEG Wait for BIOS for training.	Pull-up to VCCIO / Pull-down Platform design dependent	1Kohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1Kohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal 1 = Normal(Default) 0 = Reversed	Pull-up to VCCIO / Pull-down Platform design dependent	1Kohm
CFG[17:15]	RSVD	None	

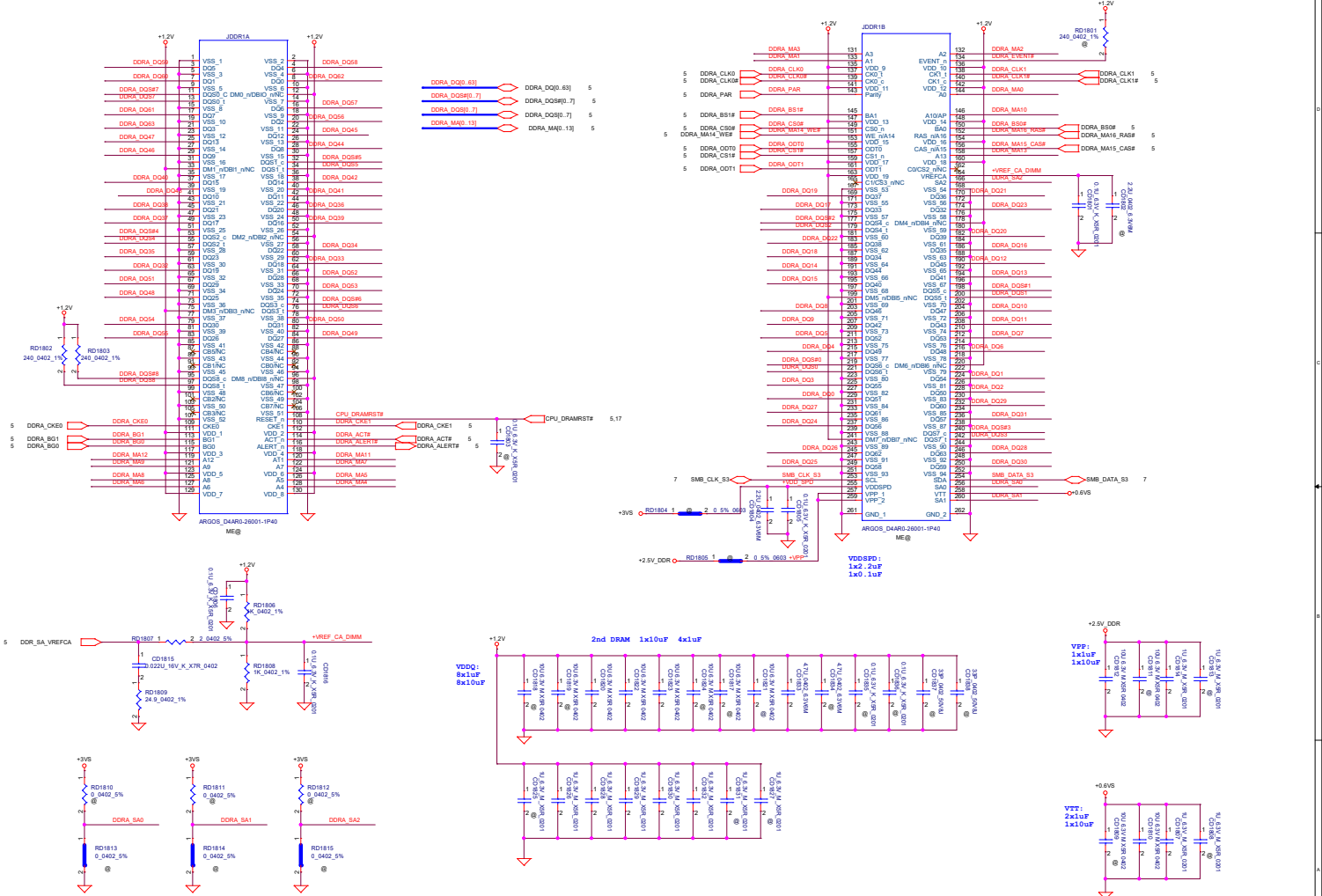
CPU PCIe Gen4 Bifurcation and Lane Reversal Mapping

Bifurcation	CFG Signals	Lanes
	CFG [14]	0 1 2 3
1x4	1	0 1 2 3
1x4(Reversed)	0	3 2 1 0



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SPD Address = A0

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N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

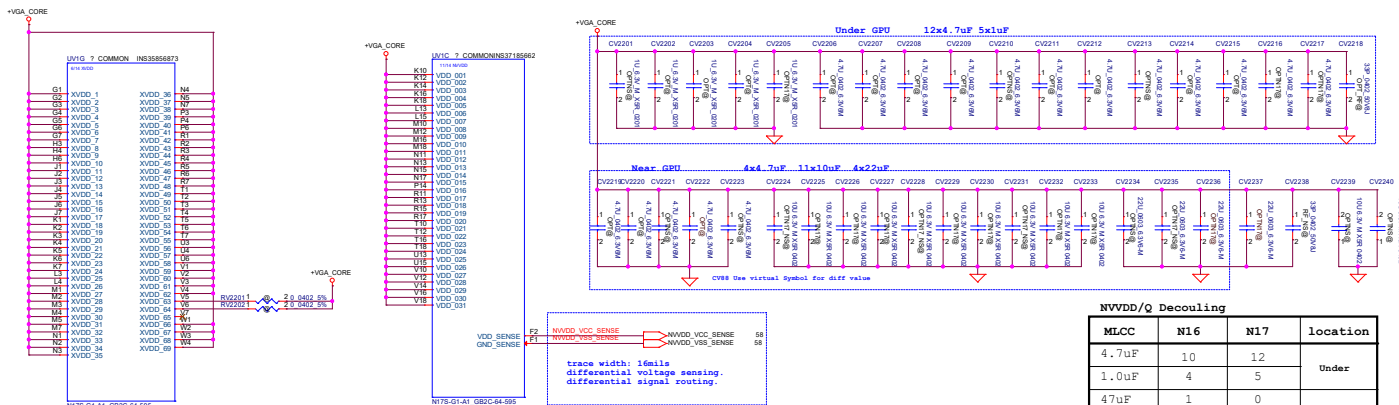
Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	NVVDD (V)	(A)	(W)	FBVDD (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

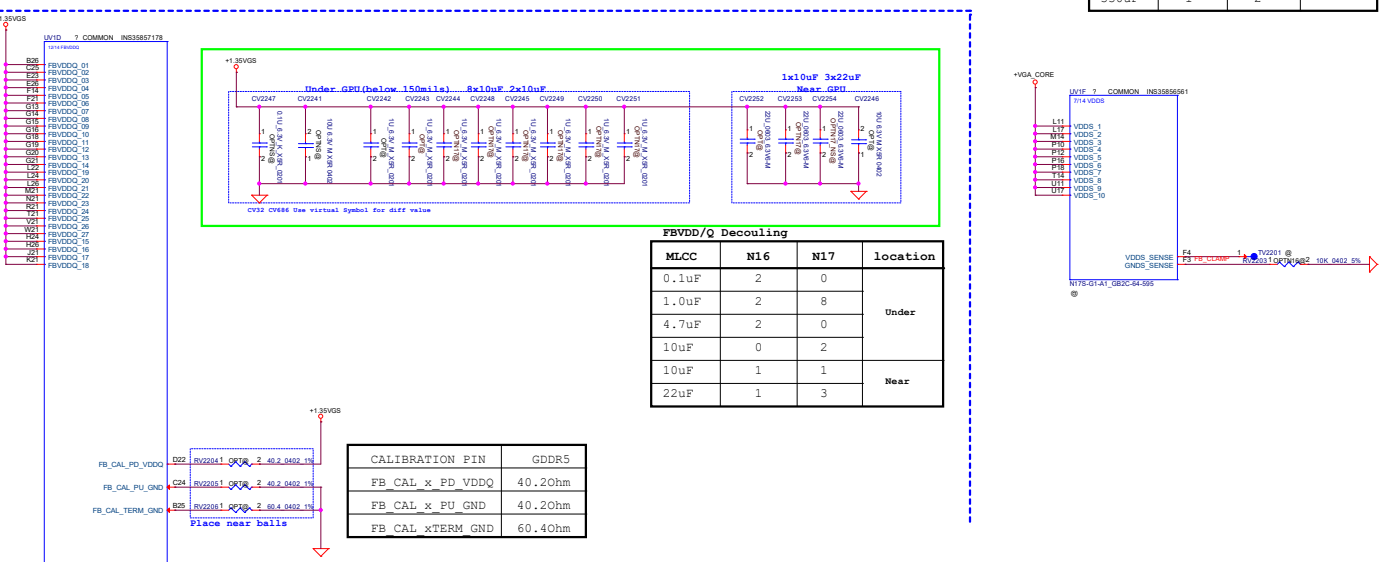
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SORJ_EXPOSED	SORJ_EXPOSED	SORJ_EXPOSED	SORJ_EXPOSED
ROM_S1	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	+3VGS	DEV1D_SEL	PCIe_CFG	SMB_ALTV_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

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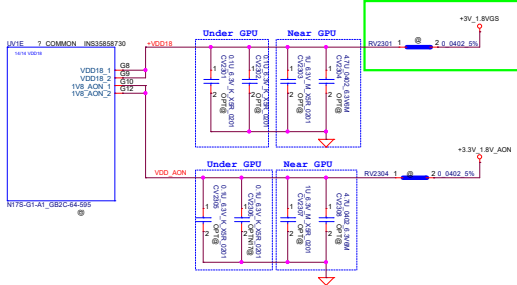
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NVDD/Q Decoupling				
MLCC	N16	N17	location	
4.7uF	10	12	Under	
1.0uF	4	5		
47uF	1	0		
10uF	0	11	Near	
22uF	1	4		
4.7uF	5	4		
330uF	1	2		



FBVDD/Q Decoupling				
MLCC	N16	N17	location	
0.1uF	2	0	Under	
1.0uF	2	8		
4.7uF	2	0		
10uF	0	2	Near	
10uF	1	1		
22uF	1	3		

CALIBRATION PIN		GDDR5
FB_CAL_x PD VDDQ	40.2Ohm	
FB_CAL_x PU GND	40.2Ohm	
FB_CAL_xTERM GND	60.40hm	



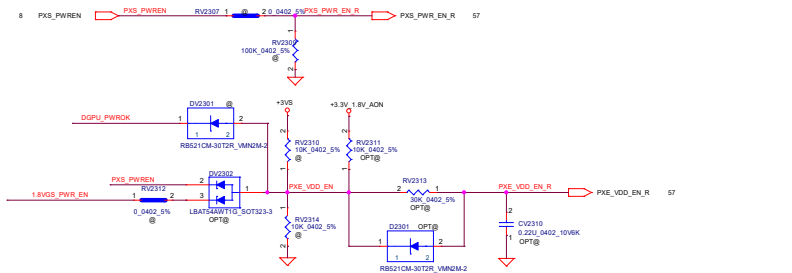
N16 3V3_MAIN(N17 VDD_18) Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	Near

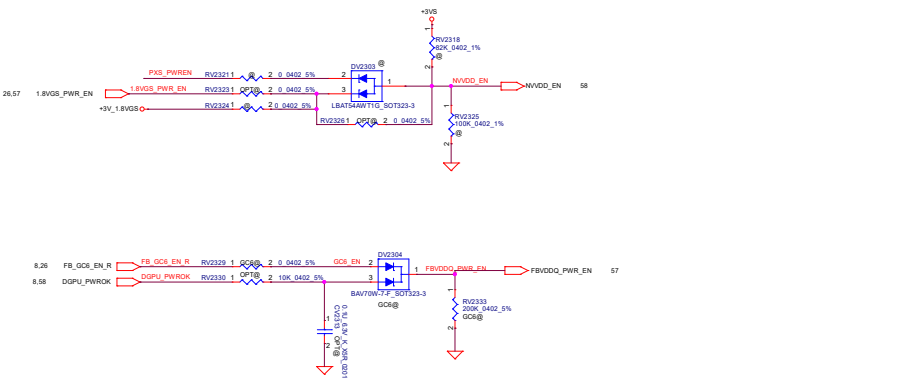
N16 3V3_AON(N17 1V8_AON) Decoupling

MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	Near

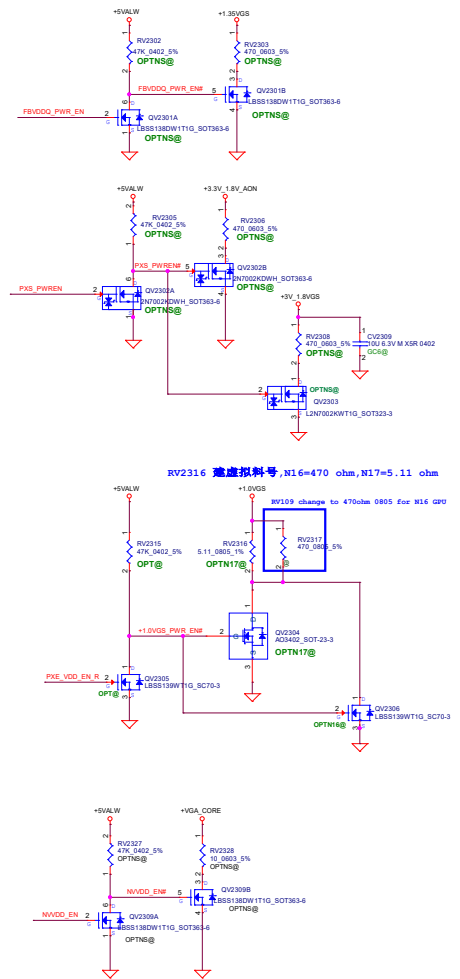
PXE_VDD & 1V8_AON



+1.8V AON TO +1.8VGS



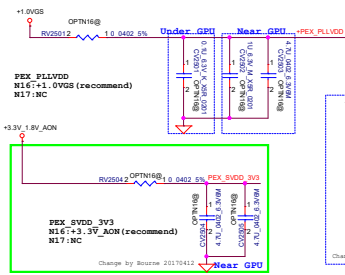
Discharge



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				Date:				Monday, November 22, 2015			

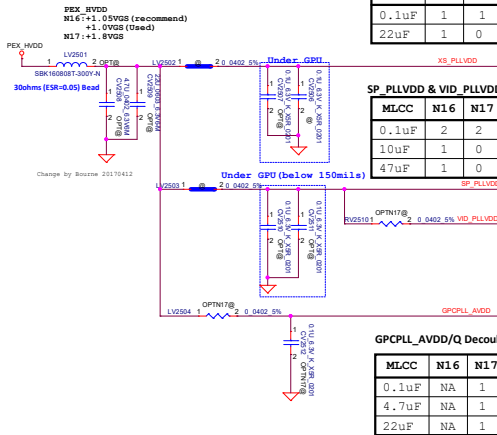
PEX_PLLVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	Near



PEX_SVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	2	NA	Near



XS_PLLVDD/Q Decoupling

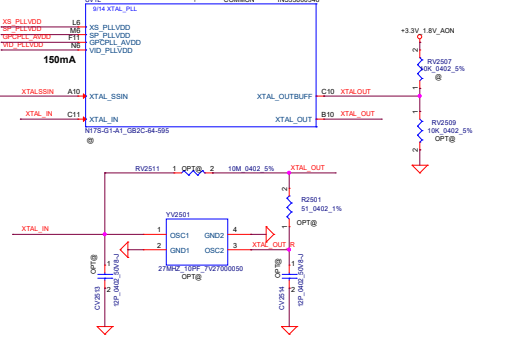
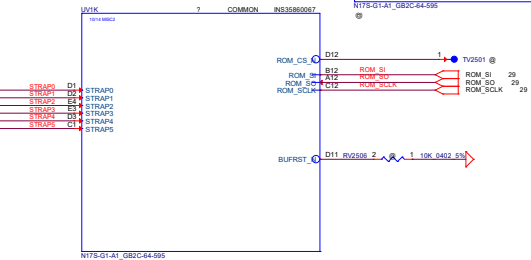
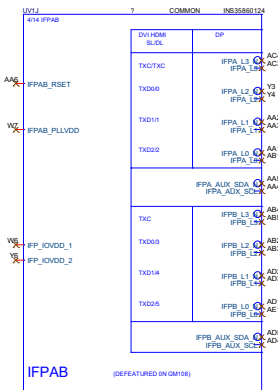
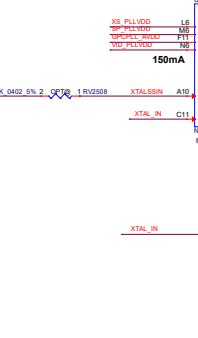
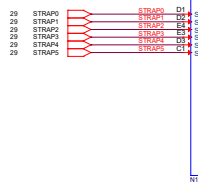
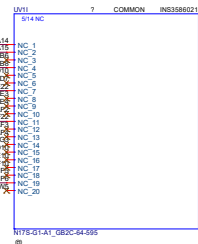
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0.1uF	1	1	Under
22uF	1	0	Near

SP_PLLVDD & VID_PLLVDD/Q Decoupling

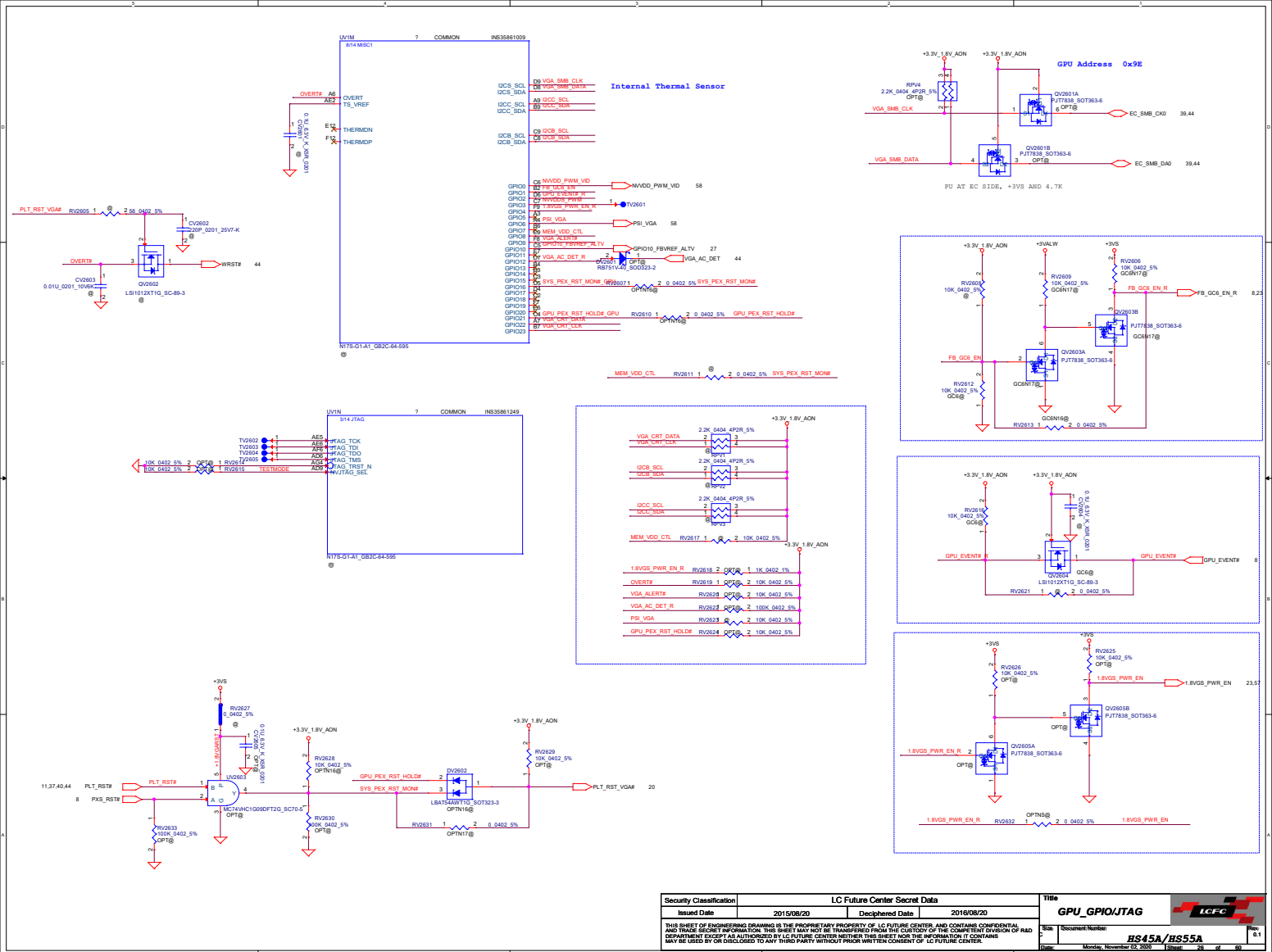
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0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	Near

GPCPLL_AVDD/Q Decoupling

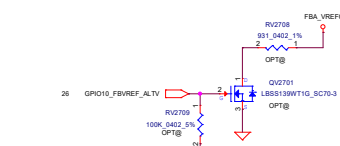
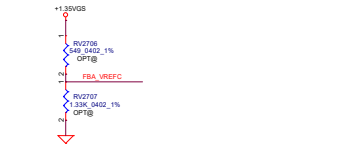
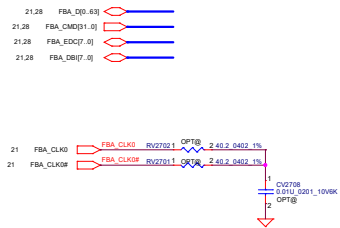
MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	Near



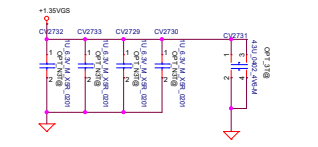
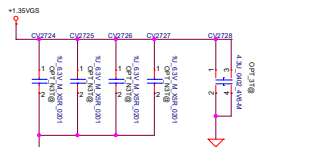
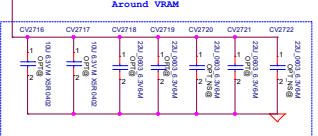
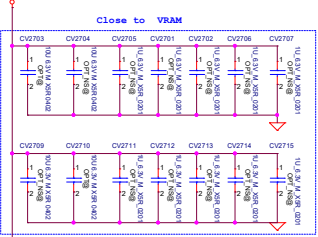
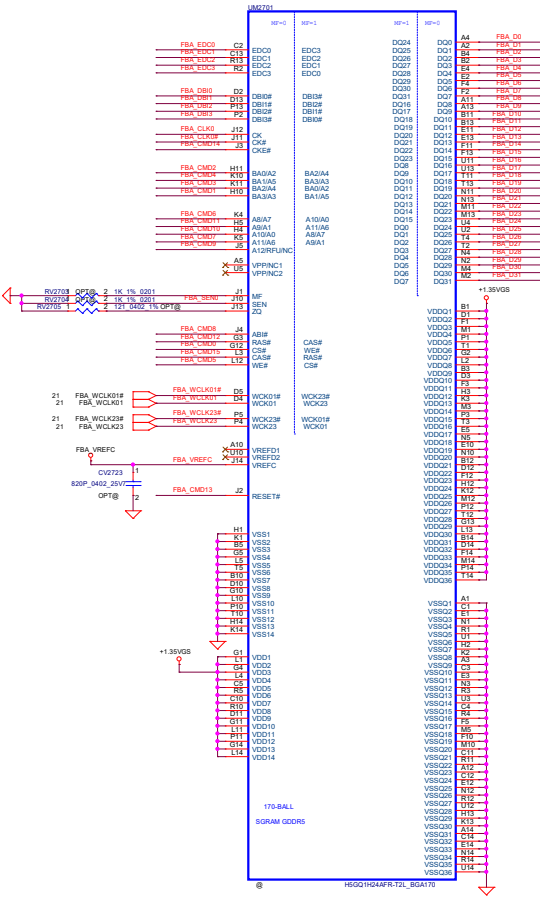
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Deciphered Date				2016/08/20				GPU_STRAP/DP/HDMI			
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25				of				80			



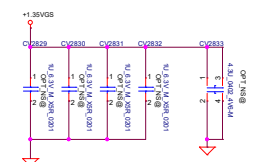
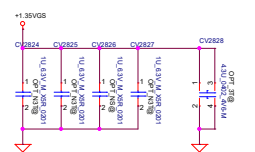
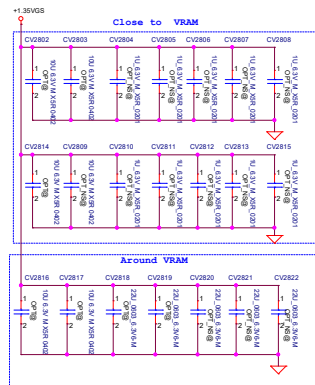
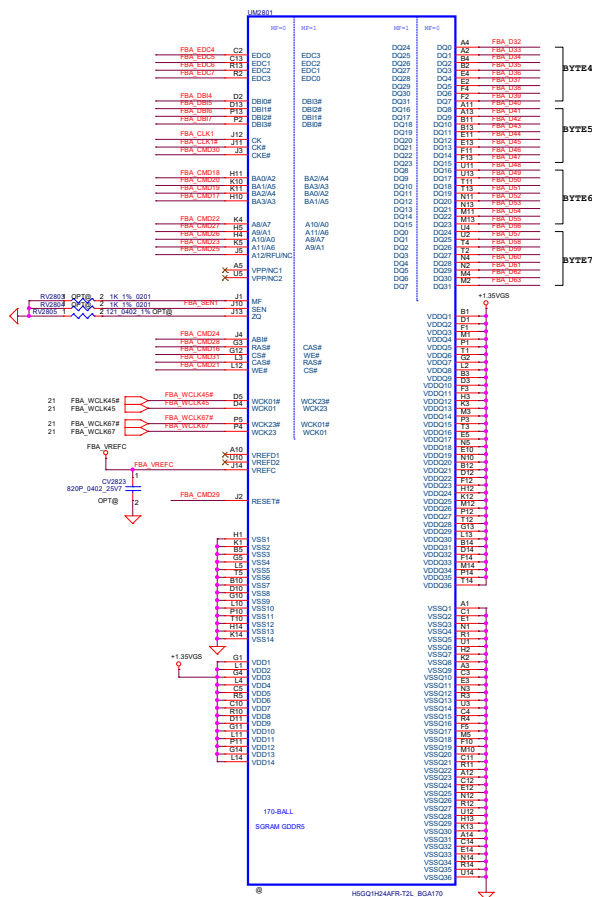
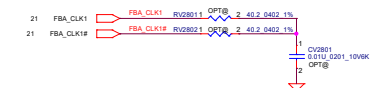
Lower 32 bits




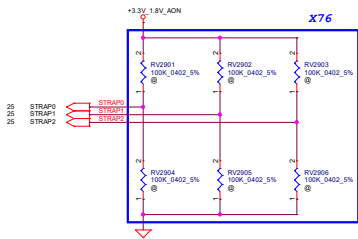
MF=0 No Mirror



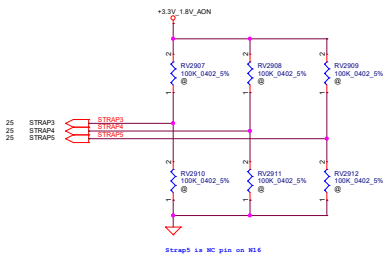
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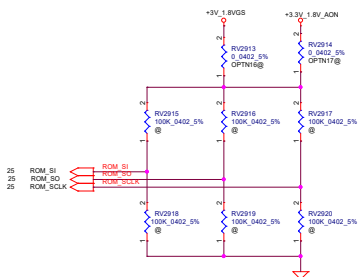


GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-NC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

- 1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE
- 1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGINAL
- 1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER
- 1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				


1:ENABLE 0:DISABLE
SOR0/1/2/3 DISABLE


DEVID_SEL
0 (Default)
1

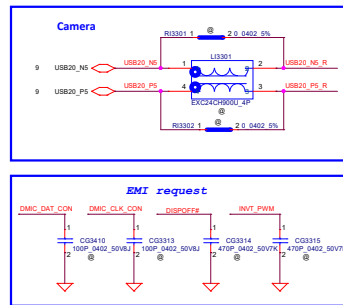
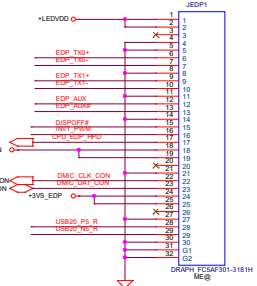
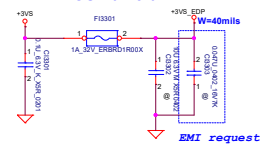
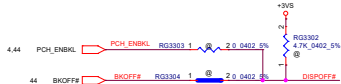
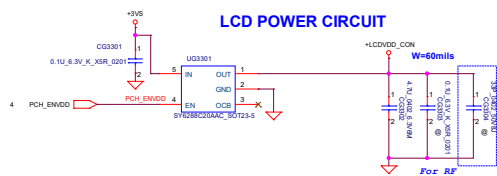
PCIE_CFG
0 (Default)
1

SMBUS_ALT_ADDR
0 0x9E (Default)
1 0x9C (Multi-GPU usage)

VGA_DEVICE
0 3D Device (Class Code 302h)
1 VGA Device (Default)

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			Issue	Monday, November 02, 2009		Sheet	02	of	00

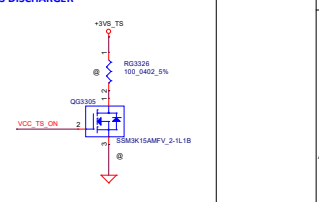
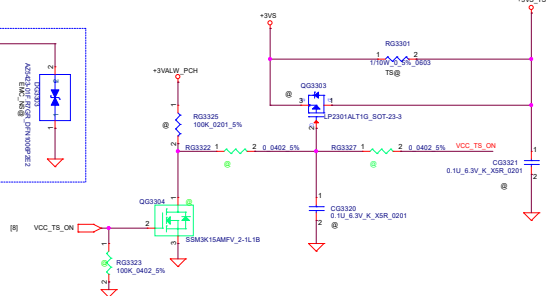
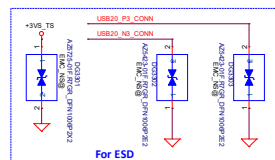




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9 USB20_N3 USB20_N3 1 3 USB20_N3_CONN

L30312 2.0 0402 5%

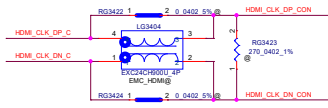
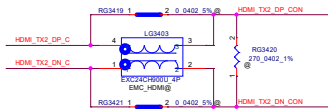
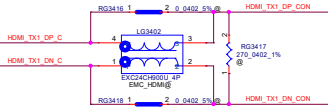
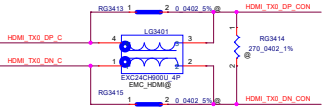
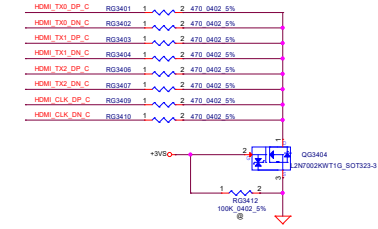
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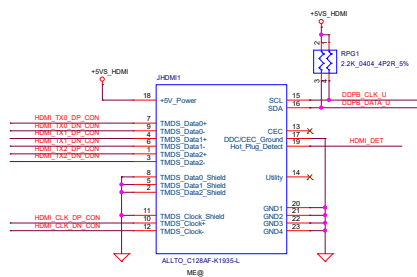
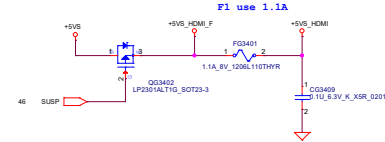
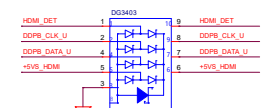
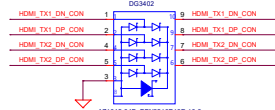
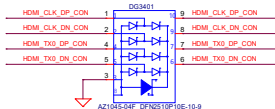
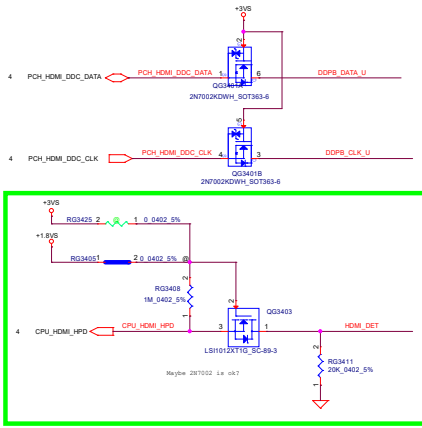
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4	CPU_HDMI_TXN2	CPU_HDMI_TXN2	Q03402	1	2	0.10 6.3V K XSR 0201	HDMI_TX2_DN_C
4	CPU_HDMI_TXP1	CPU_HDMI_TXP1	Q03403	1	2	0.10 6.3V K XSR 0201	HDMI_TX1_DP_C
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Need to change about 4700hm 5%-575412 Page115 Rev0.8



For EMC



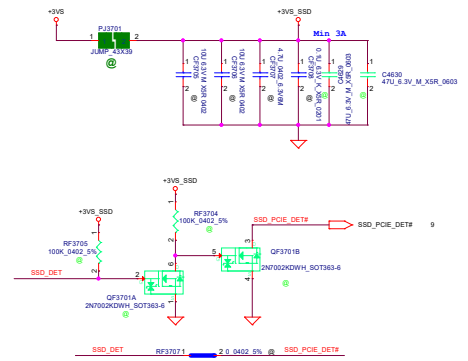
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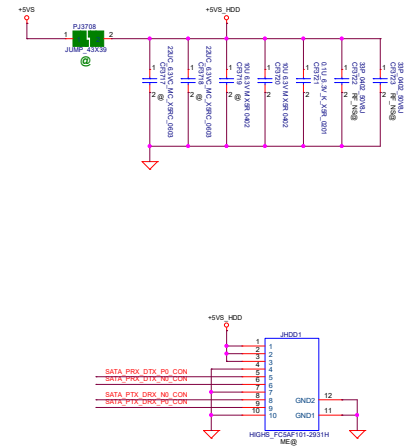



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SATA



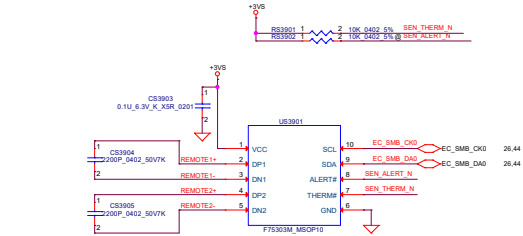
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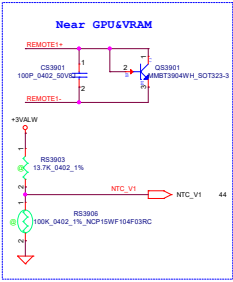
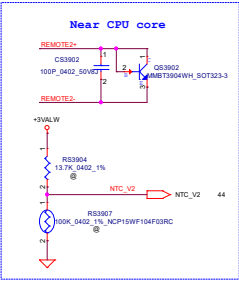
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Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	SATA HDD CONN
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				0.1
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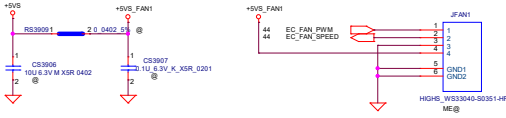
SMSC thermal sensor



REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

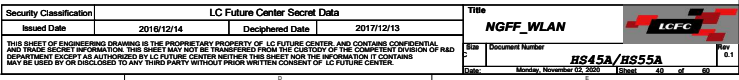


FAN Conn

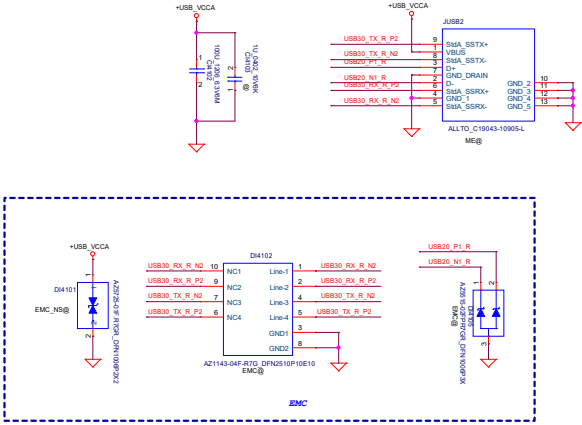
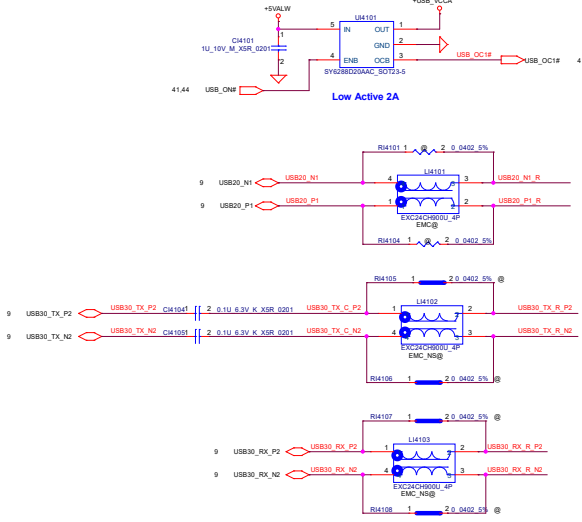


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2016/08/16		2017/08/15		LCFC	
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S/N		Document Number		Rev	
		RS45A/RS55A		8.1	
Date		Sheet		of	
Monday, November 02, 2015		99		80	

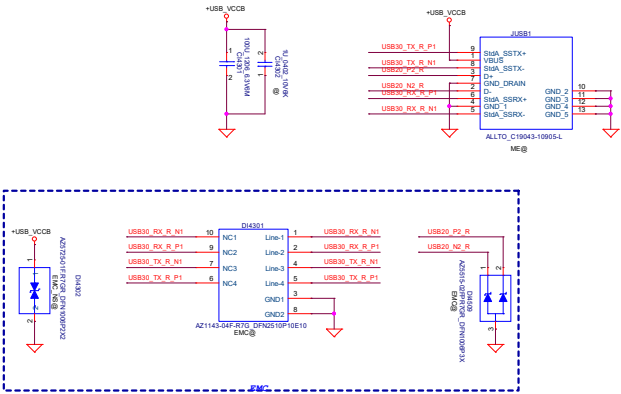
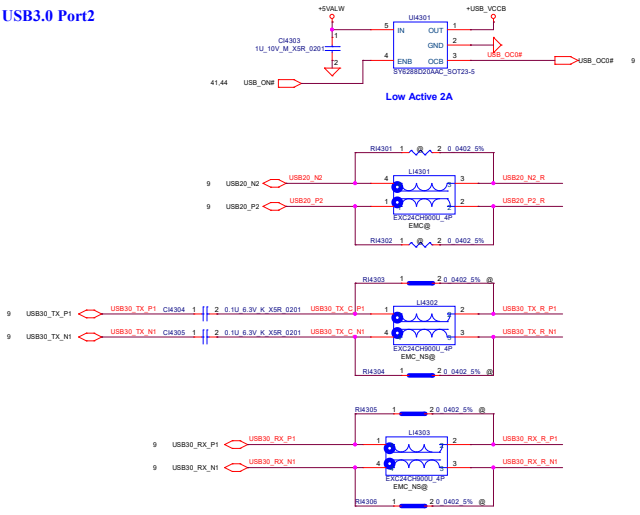
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USB3.0 Port1

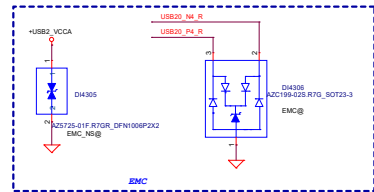
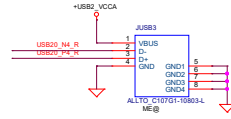
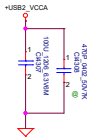
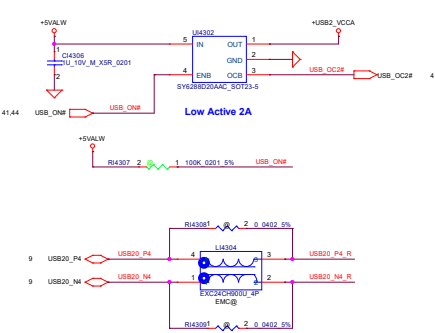


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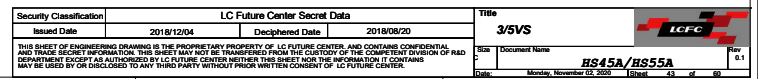


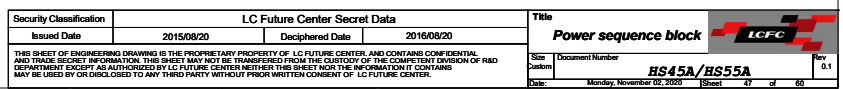
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Doc Number	RS45A/RS55A
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					8.1
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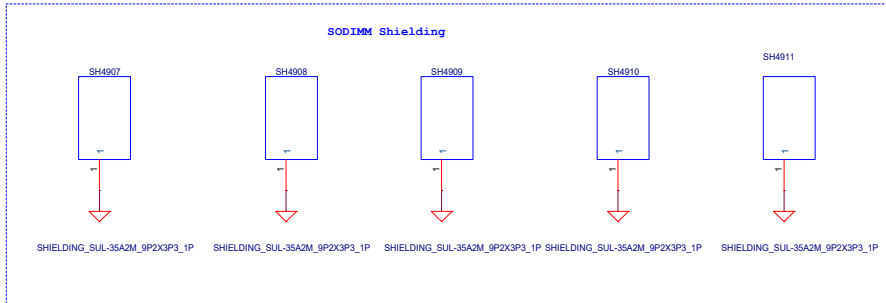
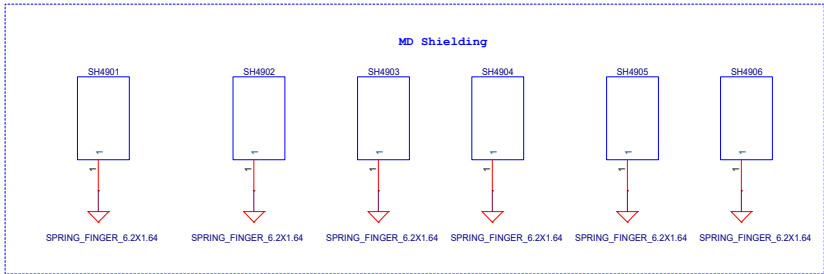
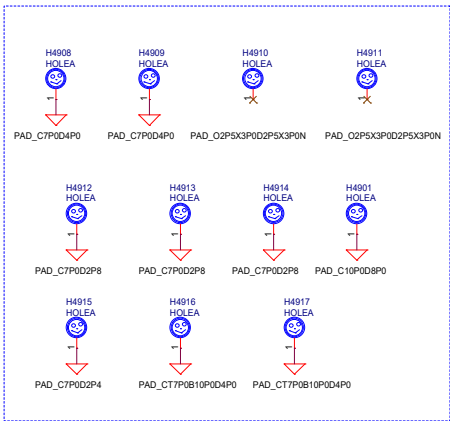
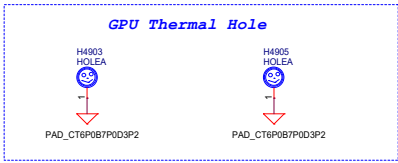
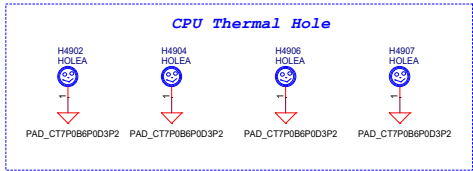
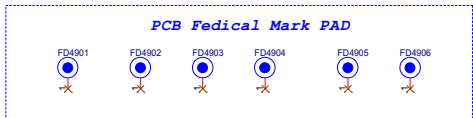
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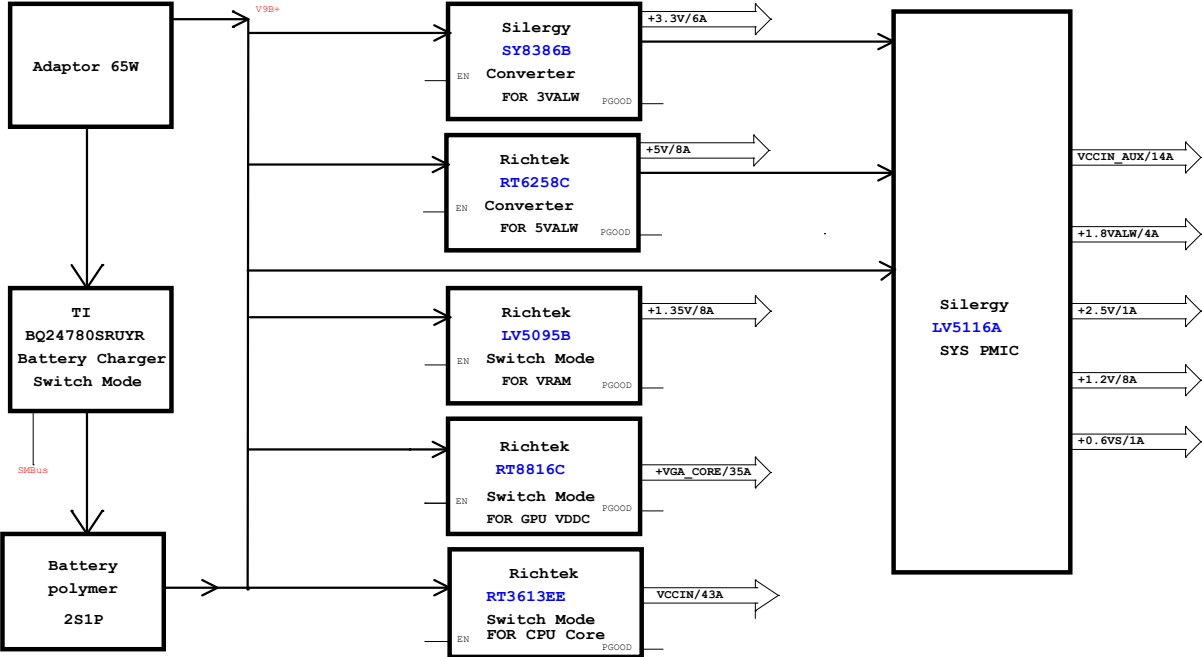
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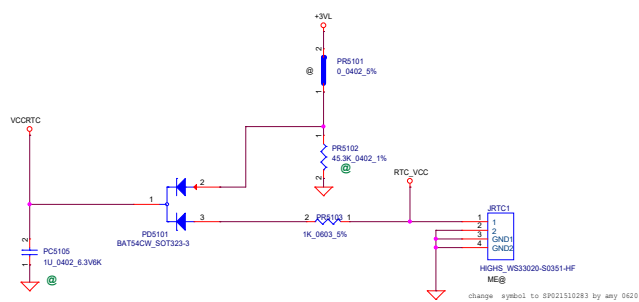
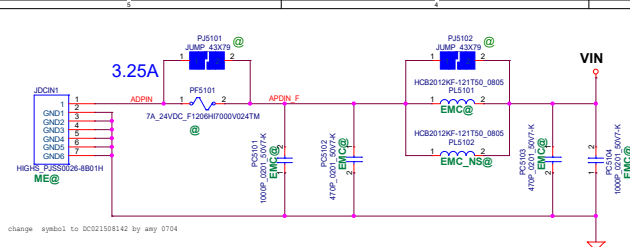





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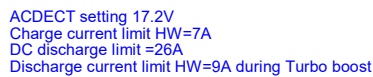



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Doc Number	RS45A/RS55A			0.1
File	Monday, November 05, 2018	Sheet	50	of 80

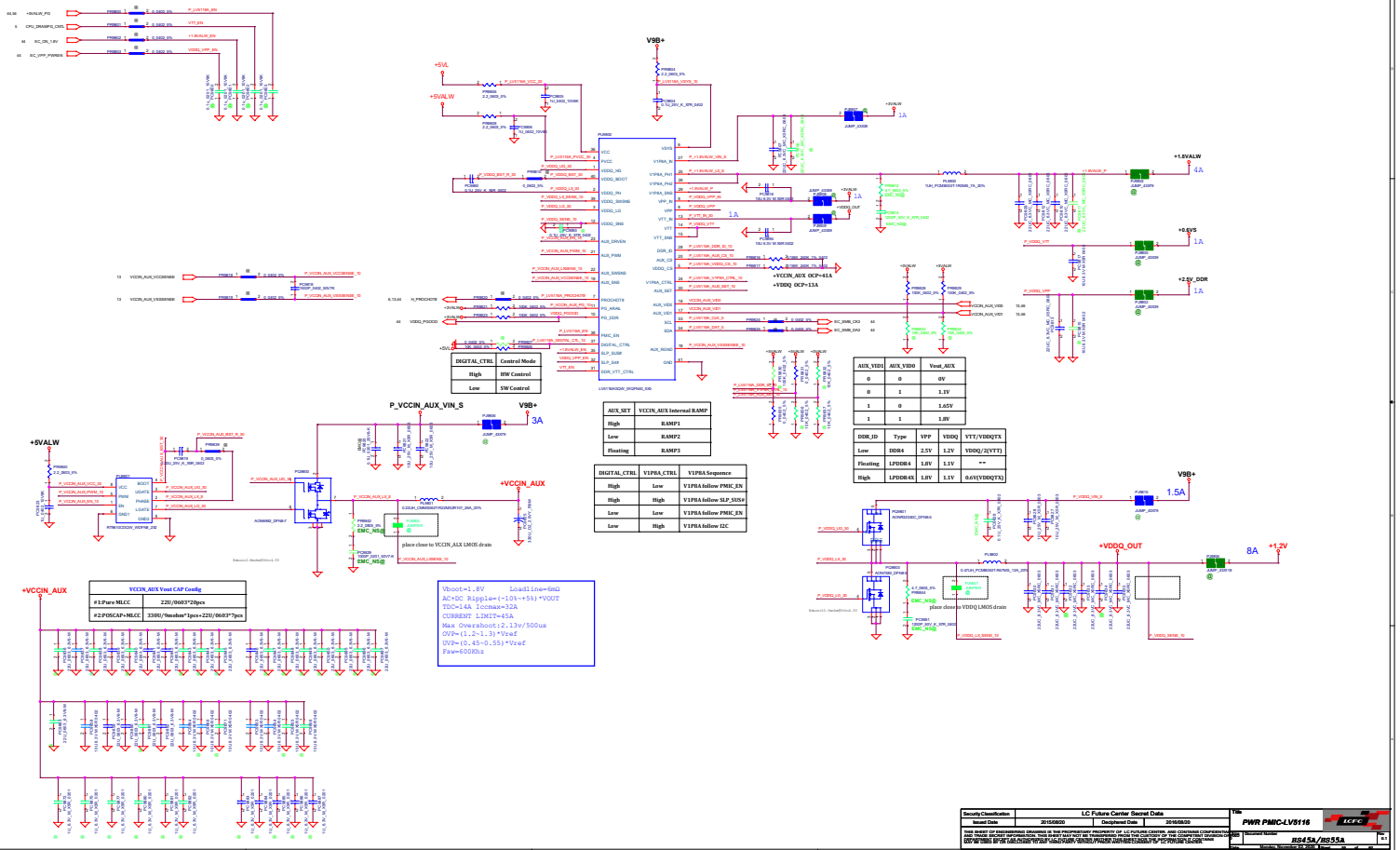


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RTC_VCC 20MIL
+3V $\overline{L}$  20MIL
VCCRTC 20MIL
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Date					Monday, November 05, 2020		Sheet 51 of 60

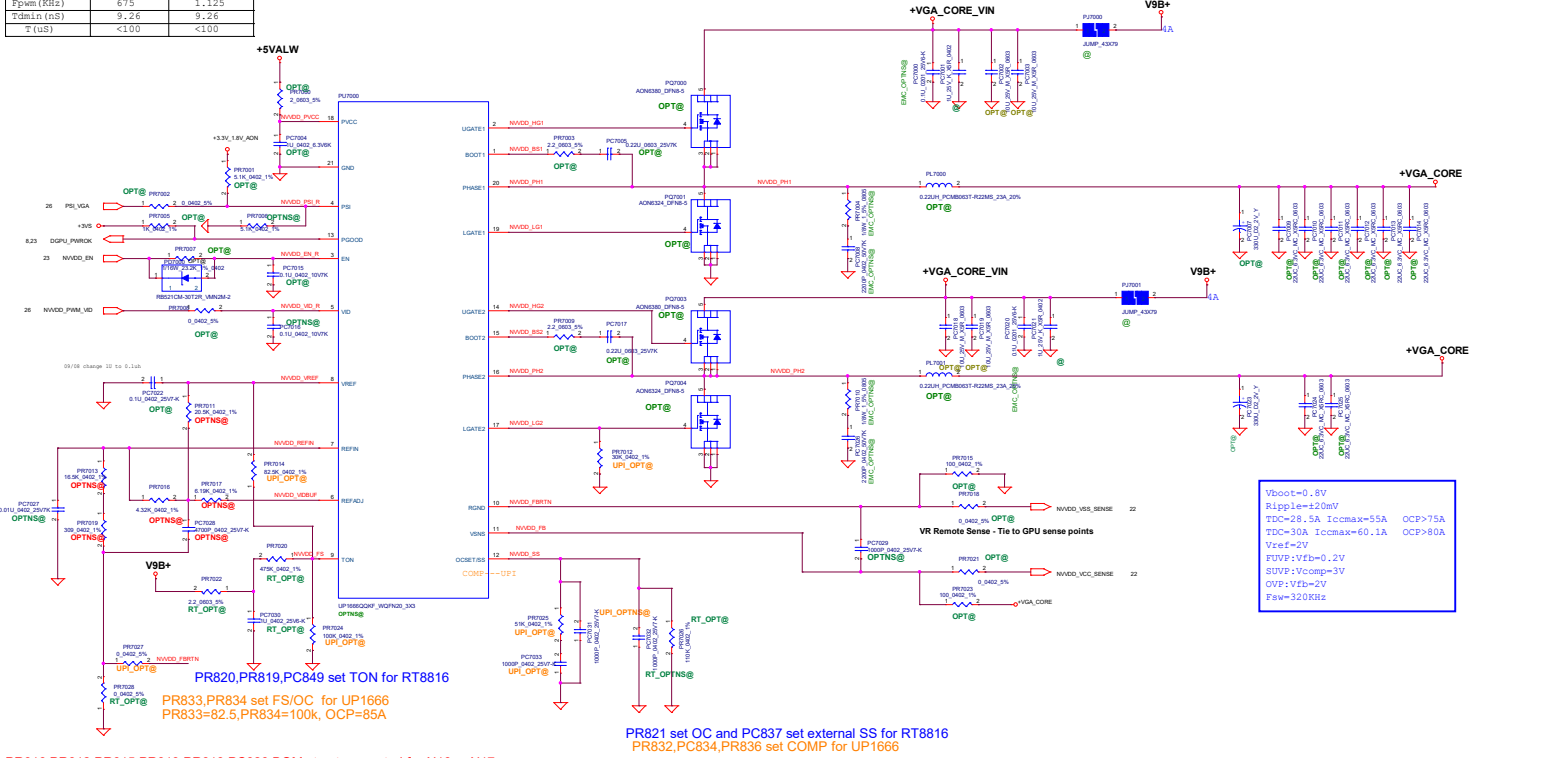


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PWM-VID Specification			
	N17 Config	N16 Config	B
Vmin(V)	0.3	0.6	
Vmax(V)	1.3	1.2	
Vboot(V)	0.8	0.9	
Vstep(mV)	6.25	6.25	
Wlevel1	160	96	
Fpwm(KHz)	675	1.125	
Tdmin(nS)	9.26	9.26	
T(uS)	<100	<100	

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM




PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1 (R2)	PR7017	6.19	2.0
R2 (R2)	PR7011	20.5	2.0
R3 (R2)	PR7016	4.32	2
R4 (R2)	PR7013	16.5	1.8
R5 (R2)	PR7019	0.309	0
C (nF)	PC7028	4.7	2.7

UPLI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

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Issued Date	20160820	Designed Date	20160820	PWR-VGA_CORE	
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Issued Date	2018/08/20	Deciphered Date	2018/08/20	POWER CHANGE LIST
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